International Journal of Engineering Research and Modern Education (IJERME)
Impact Factor: 6.525, ISSN (Online): 2455 - 4200
(www.rdmodernresearch.com) Volume 2, Issue 1, 2017

CMOS INSTRUMENTATION AMPLIFIER FOR BIOMEDICAL APPLICATIONS

R. V. Saranya* & R. Sureshkumar**

* PG Scholar, Department of ECE, Tejaa Shakthi Institute of Technology for Women, Coimbatore, Tamilnadu

** HOD, Department of ECE, Tejaa Shakthi Institute of Technology for Women, Coimbatore, Tamilnadu

Cite This Article: R. V. Saranya & R. Sureshkumar, "CMOS Instrumentation Amplifier for Biomedical Applications", International Journal of Engineering Research and Modern Education, Volume 2, Issue 1, Page Number 116-120, 2017.

Abstract:

A low power high performance CMOS instrumentation amplifier is designed through the operational amplifier (op-amp) used for biomedical applications. It consists of a low power operational amplifier with three stage op-amp structure. First two stages consists of input stage and drive stage and the third stage consist of output stage. In biomedical applications, the instrumentation amplifier (IA) requires high gain, CMRR with less noise and low power optimization. The design and analysis of the parasitic effects and the other parameters is taken and the instrumentation amplifier is found to have better performance in all aspects. With the varying width and length of the transistor, we obtain the excepted gain and CMRR. The instrumentation amplifier improves the input signal gain and CMRR to have the excepted outcome of the biomedical signal processing application. The proposed design is implemented in CMOS 180nm technology using cadence Virtuoso and the simulation is obtained through spectre simulator.

Key Words: CMOS, IA, CMRR & OP-AMP

1. Introduction:

Instrumentation amplifiers plays a very important role in many biomedical sensor readout systems where there is a need to amplify small differential signals in the presence of large common-mode interference. Most of the biomedical applications include invasive surgery robots, automotive transducers, industrial process control, linear position sensing, and bio potential acquisition systems [1-3]. Bio potential signals have less amplitude range between a small numbers of μV to mV. Since maintain a high signal to noise ratio (SNR), the input signal conditioning circuit with a very low equivalent input noise is desired. Additionally, the bandwidth of the bio potential signals range from a few tens of mHz to about 10 kHz [3]. A novel CMOS IA design based on operational amplifier [4], to achieve extremely low input referred noise without using chopper stabilization technique along with a low noise efficiency factor (NEF). In this prototype design of IA, the instrumentation amplifier provide to achieve an input referred noise of less than 1 μV in the entire bandwidth of bio-potential signals i.e. about 10 kHz [5]. However, the IA topology is adaptable and it can be optimized to meet the specific requirements of a particular measurement application. Various techniques to achieve low noise specifications in bio potential and bio-sensor amplifiers are reported [6-7]. The trends of technological development are heavily focused on improving and expanding the integration of digital processing in everyday life. This development demands that analog circuitry keep up with the phase. CMOS instrumentation amplifiers (IAs) have pumped up surprisingly for looming sensor circuit applications such as integrated strain sensors, hall sensors, thermocouples, micro electromechanical system, multichannel sensing systems and integrated bio sensors [8]. Sensors are used to translate information from various physical domains like thermal, mechanical, and magnetic to information measurable in electrical domain. This electrical signal is generally an analog signal and needs to be translated to digital signal for further signal processing. The system involved in the chain of converting the analog signal from sensors, to digital signal is called sensor readout system. In all these applications, low power consumption is aimed to reduce its cost and as battery point of view, longer operating lifetime [9].

2. Sensor Readout System:

Instrumentation amplifier models a crucial part of the low power applications since it demands to individuate noise and small amplitude signal which is desired [10]. The Transforming circuitry resides of an instrumentation amplifier which is applicable for precision amplification of DC/AC signals in differential mode while eliminating common mode signal values [11]. The Well-known design used in a low power sensor system, is an operational amplifier (Op-Amp), must manifest low power consumption and small input voltage referred noise, high Common Mode Rejection Ratio (CMRR). In this proposed work, a low voltage, low noise and high CMRR operational amplifier for portable monitoring system is described. The proposed op-amp is having an innate capacity to work under 1.8-V supply, has required design constraints like high gain & CMRR and low voltage noise [12]. Devices may pertain to different inversion region like weak, moderate and strong.

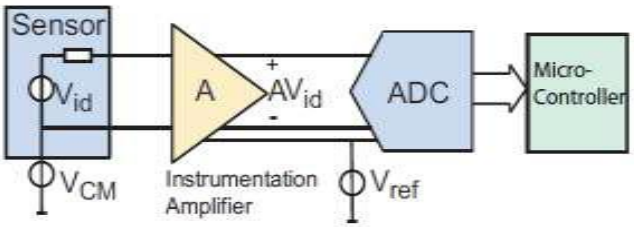

Figure 1: Block diagram of typical sensor readout system

Out of these three regions, transistor (MOSFET) functioning in saturation region is most convenient for low power applications where devices are regulated either at low voltage, current or both [13] Fig. 1 shows a typical sensor readout system whose output assumed to be in voltage. The differential voltage (Vid) from the readout system is amplified by the amplifier (A) and given to an Analog to Digital Converter (ADC). ADC converts the information to digital domain. This digital data can be processed by a micro-controller. As typical sensor signals are very small (in μV), an amplifier A is used to increase the signal before passing it to ADC. The main functions of Instrumentation Amplifier in this system are to

- ✓ Amplify the differential voltage (Vid).
- ✓ Reject the sensor common mode voltage (VCM).
- ✓ Level shift to ADC reference voltage (Vref).

As these amplifiers are used to detect very small input differential signals, the input referred errors (due to offset & noise) of such amplifiers should be well below the minimum input signal.

3. Instrumentation Amplifier:

Instrumentation amplifier can be designed from an op amp circuit but the behavior of instrumentation amplifier is intensely different than an op-amp and difficult to design precisely from single op-amp circuit. Instrumentation amplifier can be designed by several different ways. The commonly used techniques are difference amplifier, two op-amps, three op-amps, switched capacitor, capacitive coupled, current mode, resistive feedback and current feedback instrumentation amplifier. The classical three op-amp instrumentation amplifier [14] having inputs VIN- & VIN+ defined by the input polarity of difference amplifier A3. These inputs can be categories as common mode voltage and difference voltage. Standard instrumentation amplifier using a unity gain difference amplifier in the output stage, however, can limit the input common mode range significantly [15]. The three op-amp IA suffers from a limited Common Mode Rejection ratio (CMRR) due to resistor mismatch. It does not provide a good power noise tradeoff a switched-capacitor IA can be used to improve the CMRR, but it suffers from low input impedance. A CFIA can achieve better CMRR and input impedance as compared to three op-amp and Switched Capacitor IA.

Our main concern while designing an IA is to reduce the interferences in the form of common mode voltage. The block diagram of proposed complete IA shown in fig. 2.The two stage op-amp includes a bias circuit, a differential amplifier, a second gain stage and a compensation circuit [16]. The differential amplifier stage provides gain to improve the performance in terms of noise and offset. The bias circuit is used to establish the operating point for all transistors in saturation as well as sub-threshold region. The main motto of compensation circuit is to maintain the stability when negative feedback is applied to the op-amp.

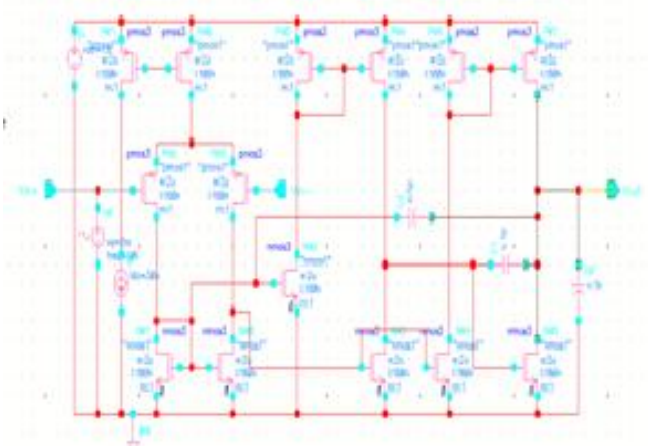

Figure 2: Schematic diagram for three stage amplifier instrumentation

4. Simulation Results and Discussion:

AC analysis has been done for the proposed IA circuit using cadence spectre tool in CMOS 180nm technology. By using this analysis gain, phase response, magnitude response as well as the trans conductance are measured. Fig. 7 shows the magnitude response and Fig.4 shows the gain of proposed instrumentation amplifier.

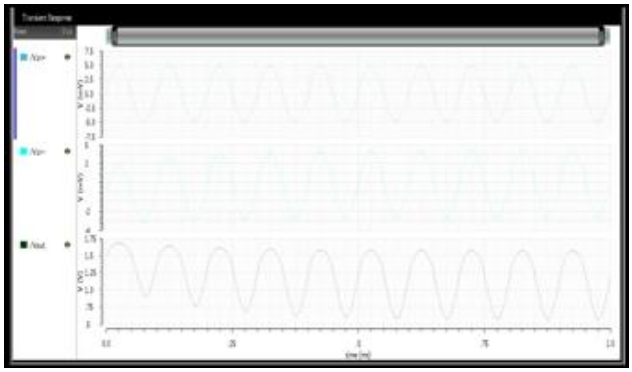

Figure 3: Transient response of three stage Instrumentation amplifier

Transient response of three stage instrumentation amplifier is shown in Fig 3.Input voltage given to the circuit is 5mV.The amplified output is 1.5V. Simulation result of gain in 10dB shown in Fig 4.Output gain at 10dB is 17.7dB.

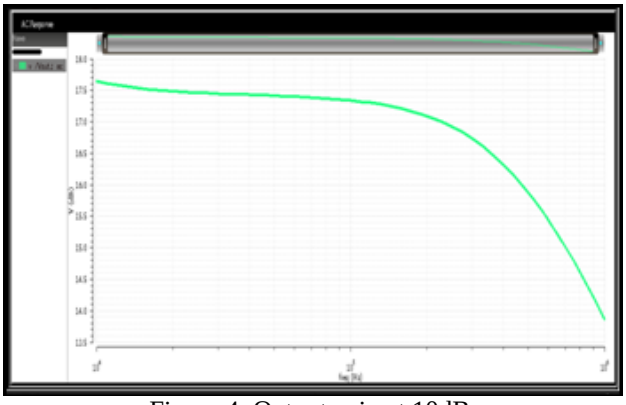

Figure 4: Output gain at 10dB

Gain in 20dB shown in Fig 5. Output gain at 20 dB is 37dB.

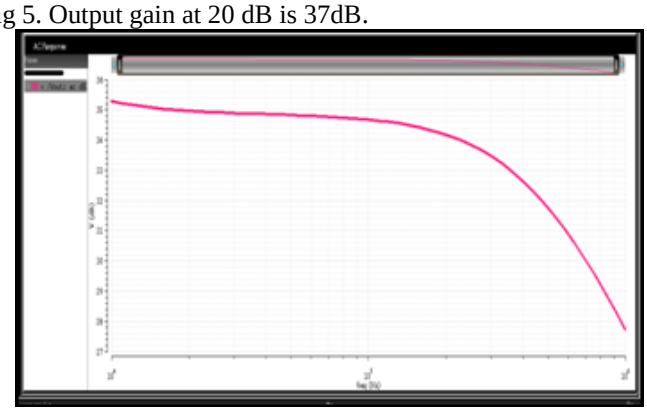

Figure 5: Output gain at 20dB

Trans conductance of instrumental amplifier shown in Fig 6.

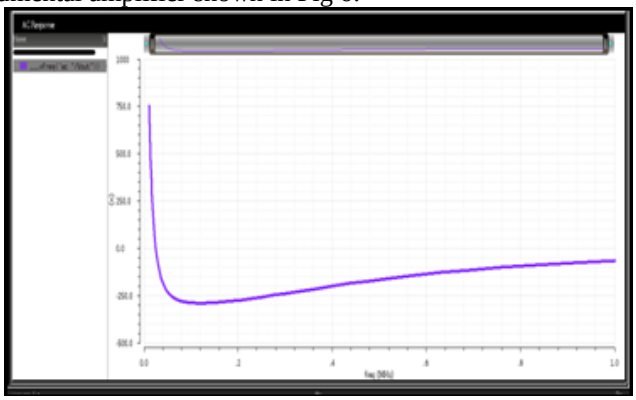

Figure 6: Trans conductance of instrumental amplifier

Figure 7 & 8 shows the magnitude & phase response. Magnitude response of instrumentation amplifier is 58V. Phase response of instrumental amplifier is -7deg.

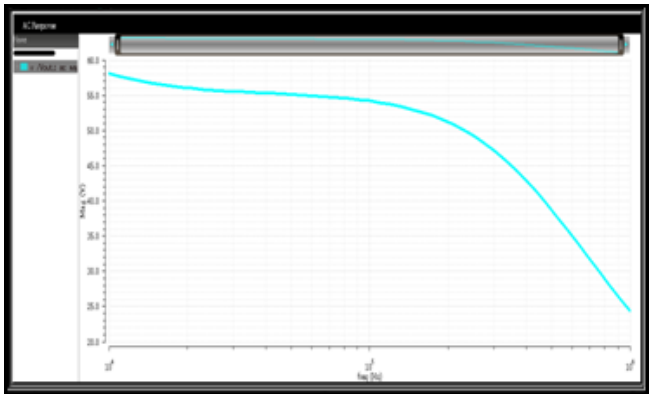

Fig 7: Output for magnitude response

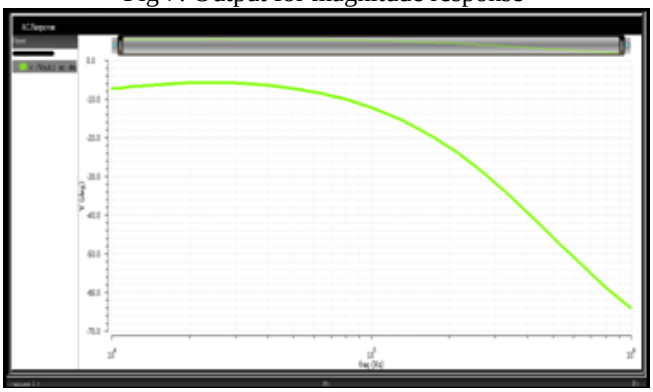

Fig 8: Output for phase response

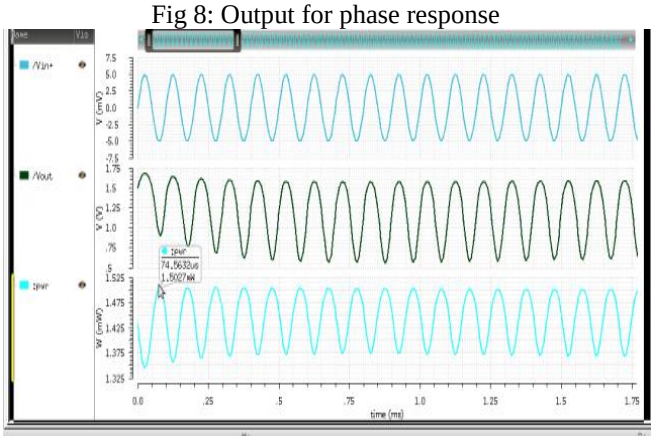

Fig 9: Power of instrumentation amplifier

Fig 9 shows the power of instrumentation amplifier. The maximum power of instrumentation amplifier is found to be 1.5027nW

5. Conclusion:

The main aim of the proposed architecture is achieved using three stage op-amp. A simulation result of gain was taken and CMRR was found to be high. The gain, trans conductance, phase and magnitude response were taken using the Cadence virtuoso. The proposed architecture was designed in CMOS180nm technology and this architecture ensured moderate noise and power which is one of the vital circuit applications.

6. References:

1. B. D. Miller and R. L. Sample, "Instrumentation amplifier IC designed for oxygen sensor interface requirements," IEEE J. Solid-State Circuits, vol. 16, no. 6, pp. 677–681, Dec. 1981.
2. V. Schaffer, M. F. Snoeij, M. V. Ivanov, and D. T. Trifonov, "A 36 V programmable instrumentation amplifier with sub-20 V offset and a CMRR in excess of 120 dB at all gain settings," IEEE J. Solid-State Circuits, vol. 44, no. 7, pp. 2036–2046, Jul. 2009.
3. J.-M. Redouté and M. Steyaert, "An instrumentation amplifier input circuit with a high immunity to EMI," in Proc. 2008 Int. Symp. Electromagn. Compatibility—EMC Eur., Hamburg, Germany, Sep. 2008, pp. 1–6.
4. N. Thakor, Biopotentials and Electrophysiology Measurement, CRC Press, Boca, Raton, USA, 1999.

5. S. Joshi, V. Thaker, A. Amaravati, M. Shojaei-Baghini, Low-power low-noise analog signal conditioning chip with on-chip drivers for healthcare applications, Microelectron. J. 43 (2012) 828–837.
6. O. Cota, D. Plachta, T. Stieglitz, Y. Manoli, M. Kuhl, In-vivo characterization of a 0.8 3 - µVrms input-noise versatile CMOS pre-amplifier, in: 2015 7th International IEEE/EMBS Conference on Neural Engineering (NER), pp. 458–461
7. R. Harrison, C. Charles, A low-power low-noise CMOS amplifier for neural recording applications, IEEE J. Solid-State Circuits (2003).
8. Ong, Geok Teng, and Pak Kwong Chan. "A Power-Aware Chopper-Stabilized Instrumentation Amplifier for Resistive Wheatstone Bridge Sensors", IEEE Transactions on Instrumentation and Measurement, 2014.
9. Qinwen Fan, Johan H. Huijsing and Kofi A. A. Makinwa, A 21 nV/ √HZ Chopper-Stabilized Multi-Path Current- Feedback Instrumentation Amplifier With 2µV Offset" IEEE Journal Solid State Circuits, Vol. 47, No. 2, pp. 464- 475, February2012
10. Joachim H. Nagel, "Biopotential Amplifiers", the biomedical engineering handbook: Second Edition. Ed. Joseph D. Bronzino Boca Raton: CRC Press LLC, 2000
11. C. Kitchin and L. Counts, "A designer's guide to Instrumentation Amplifiers", 3rd edition, Analog Devices, pp. 10-25, 2006.
12. K.K. Rajput, A.K. Saini and S.C. Bose, "DC Offset Modeling and Noise Minimization for Differential Amplifier in Subthreshold Operation", IEEE annual symposium on VLSI, pp. 247-252, 2010.
13. Thomas Kugelstadt, "Getting the most out of your instrumentation amplifier design", Analog Applications Journal, Texas Instruments Incorporated, Texas, USA, pp. 25-30, 2005.
14. J. Dangi and R.C. Gurjar, "An ECG Instrumentation Amplifier with improved CMRR and Gain using 180nm technology", IEEE Conference, pp. 92-95, June 2014.
15. A. Goel and Gurmohan Singh, "Novel high Gain low Noise CMOS Instrumentation amplifier for biomedical applications", IEEE International conference on Machine Intelligence and Research Advancement, pp. 392-396, 2013.
16. Chih-Jen Yen, Wen-Yaw Chung and Mely Chen Chi , "Micro-Power low offset Instrumentation Amplifier IC Design for Bio-Medical System Applications", IEEE Transactions On Circuits And Systems-